

1

2

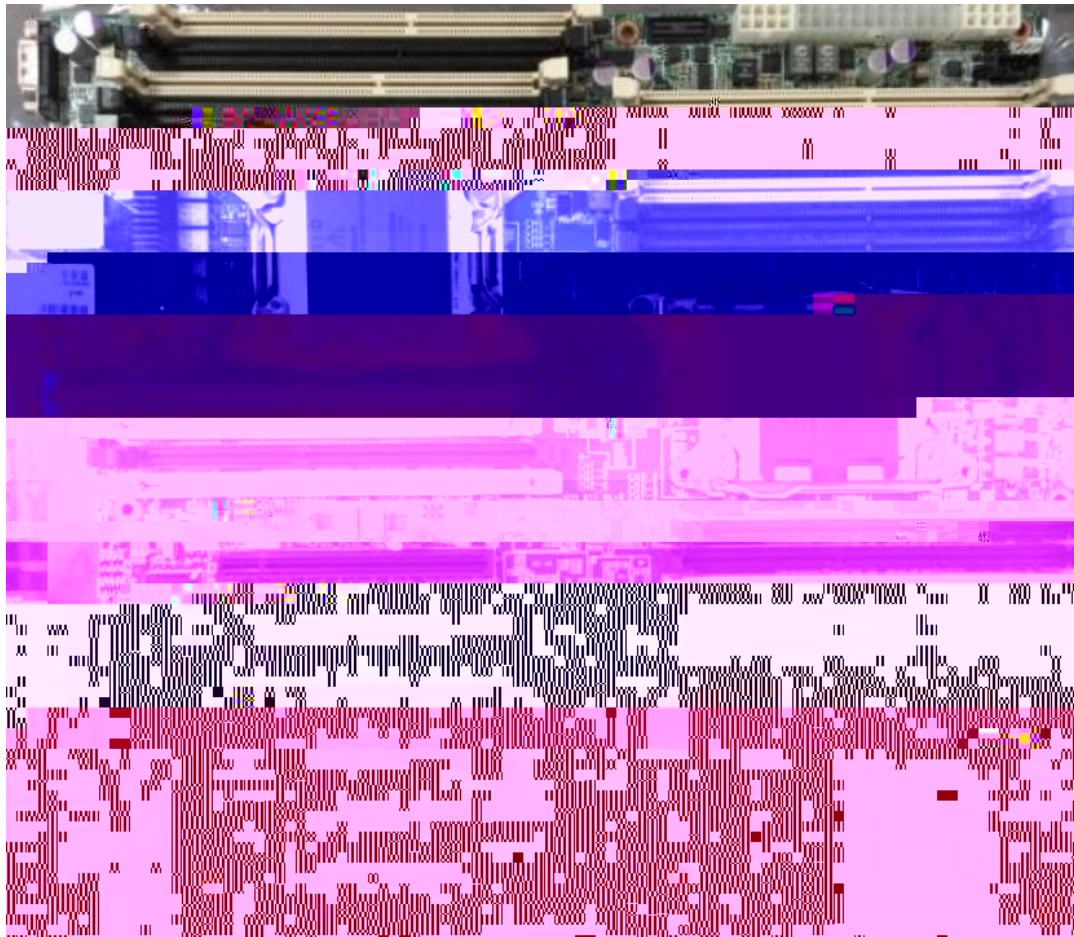
2.1

V1 V2



2.2 V1

2.2.1 V1



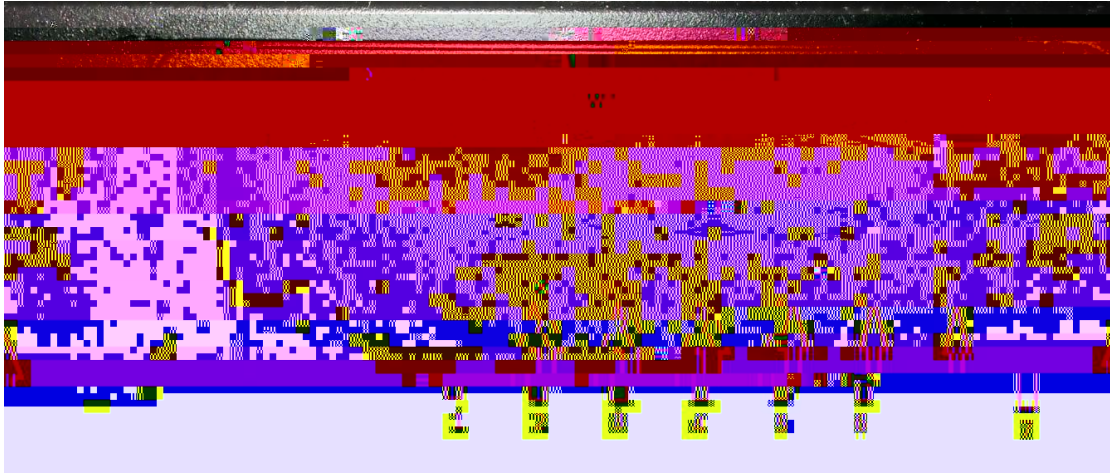
2.2.2 V1

2.2.3 CPU

2.2.4 CLR_CMOS

S
S

2.2.5

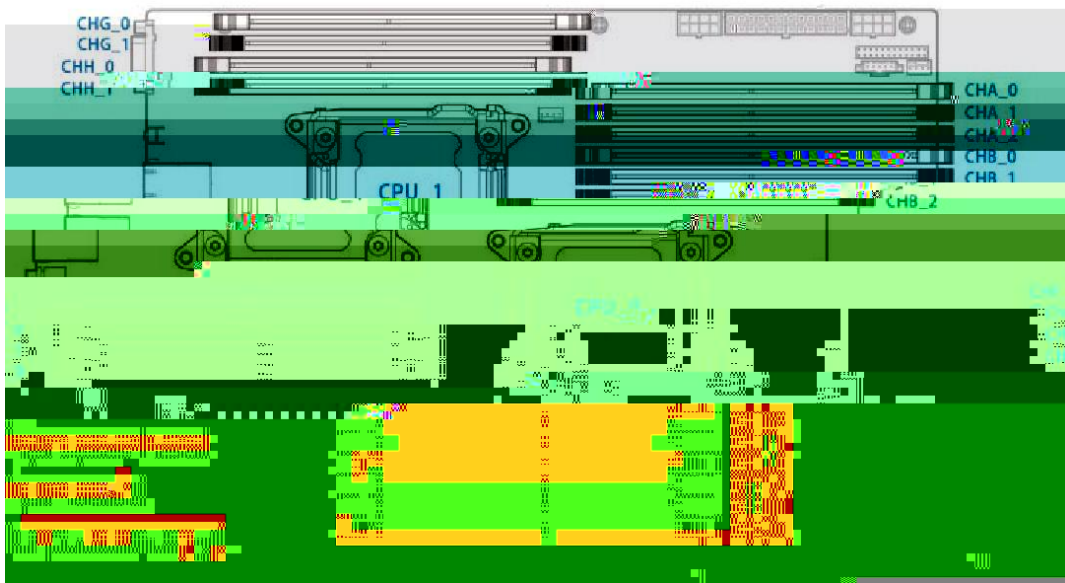


2.3 V2

2.3.1 V2

	()
	S
	S

2.3.2 V2



:
 :
 CHB_1/CHC_1/CHD_1/ CHA_2/ , ,

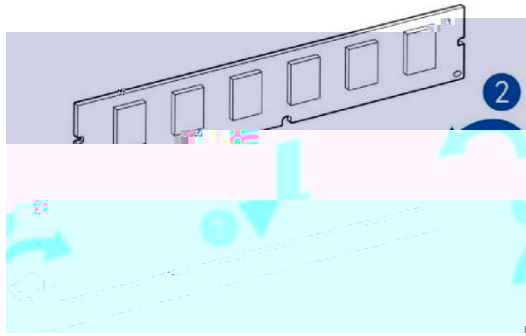
CHD_0, CHA_1 , ,

''

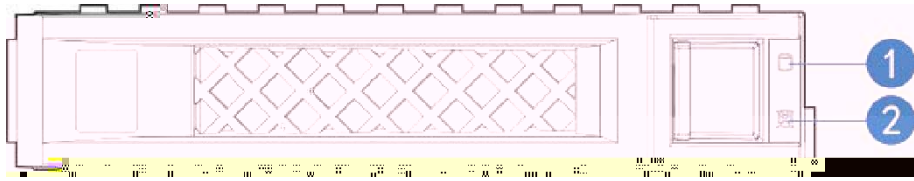
1:

2:

,



2.3.3



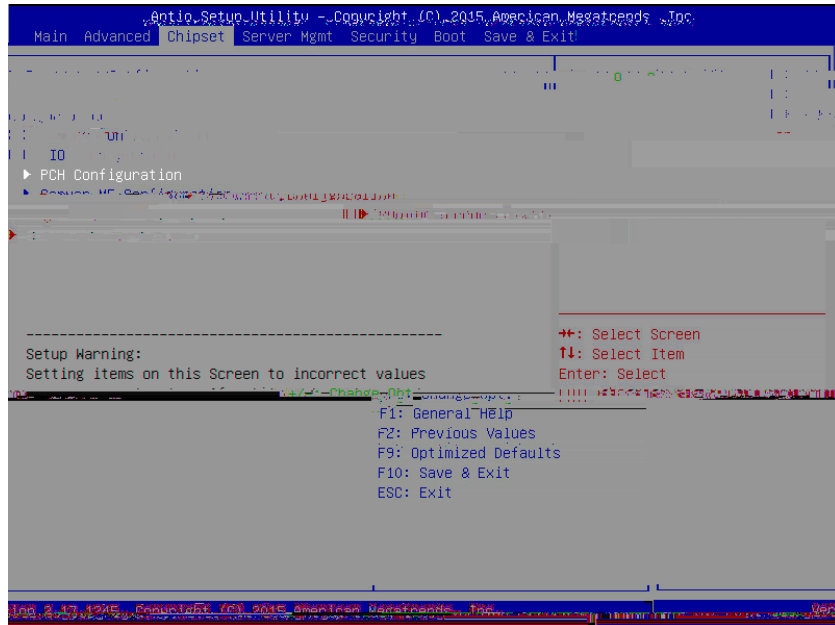
3.1.2



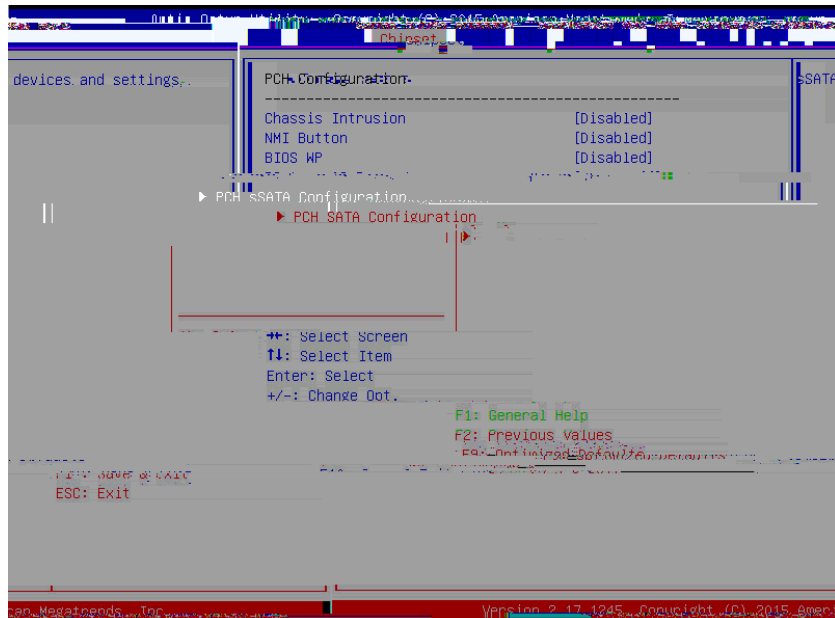
3.2.2

S

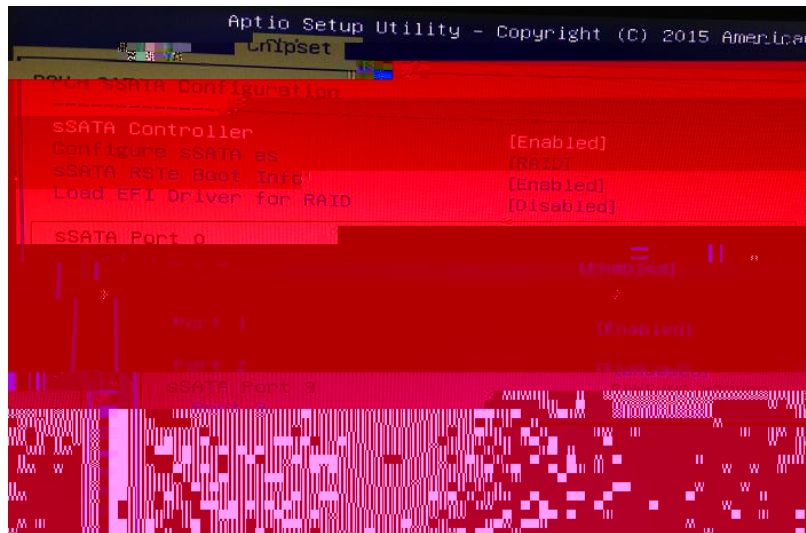
S S



S



S



S

3.4.2

S

3.5

3.5.1

S

3.5.2

3.6

3.6.1

3.7.2

S

S

B

4

